Claims

1. A method for improving digital testing of an analogue or mixed-signal circuit, the method comprising optimising an input digital test signal.

2. A method as claimed in claim 1, wherein the step of optimising comprises applying a plurality of different digital inputs to a fault free circuit and a faulty circuit, preferably software-based simulations of the fault free and faulty circuits; monitoring the corresponding outputs of the fault free and the faulty circuits for each input, and using the fault free and the faulty outputs for each input to select an improved test input as part of an optimisation procedure.

3. A method as claimed in claim 2 comprising for each input, determining a measure, for example a figure of merit, that is indicative of differences between the output of the fault free circuit and the output of the known faulty circuit in response to the digital input signal and selecting an improved input test signal based on the determined measures for all of input digital signal.

4. A method as claimed in claim 2 or claim 3, wherein the step of applying a plurality of digital input signals involves applying an initial signal and then varying that according to pre-determined criteria.

5. A method as claimed claim 4, wherein the step of varying the initial input digital signal involves changing the length of one or more individual pulses in that signal.

6. A method as claimed in claim 5, wherein the length of individual pulses is varied by the same amount or by increasingly large or small amounts or by different amounts, which different amounts may be selected randomly or according to predefined criteria.

7. A method as claimed in claim 6, wherein the length of all of the pulses is varied by the same amount in sequence one after the other.

8. A method as claimed in claim 7 further involving changing the size of the amount by which the pulse lengths are varied and repeating the process of varying.

9. A method as claimed in any of claims 4 to 8, wherein the process of varying the input digital signal involves applying a pre-determined function to the input sequence, such as a pattern shift function, which function in effect modifies simultaneously all pulses in the input pattern at once.

10. A method as claimed in any of claims 2 to 9 comprising applying a range of different initial digital inputs, each of these being varied according to pre-determined criteria to find a local optimum for each initial input.

11. A method as claimed in claim 10 comprising comparing all of the local optima and selecting the optimum signal.

12. A method as claimed in any of claims 2 to 11, wherein the output signals used for each of the fault free circuit and the known faulty circuit are analogue outputs.

13. A method as claimed in claim 12, wherein the analogue output signals are processed to prevent domination of large differences in the output prior to selection of the optimum input signal.

14. A method as claimed in claim 13, wherein processing of the analogue signals involves using a function having an output that saturates at two different predetermined values for extreme negative and positive values of input.

15. A method as claimed in claim 14, wherein the function is a sigmoidal function, which employs a non-linear squashing function based on the sigmoid or logistic equation, wherein preferably the sigmoidal function is a hyperbolic tan function.

16. A method as claimed in any of claims 1 to 11, wherein digital outputs from the fault free and the faulty circuits are used to determine the optimum digital input signal.

17. A method as claimed in any of the preceding claims, wherein a fault detection ratio is used to determine the optimum circuit, this being defined as the proportion of a set of predefined faults that can be detected according to a set of criteria for fault discrimination.

18. A method as claimed in any of claims 3 to 17, wherein the figure of merit is the Hamming distance between the digital output response for the fault free circuit and the output response for the faulty circuit.

19. A method as claimed in claim 18, wherein the figure of merit is proportional to or a function of the Hamming distance.

20. A method as claimed in any of the preceding claims, wherein an exhaustive evaluation of a pre-determined group of possible digital sequences is used to find one or more good initial or starting digital input sequences.

21. A method as claimed in any of claims 2 to 20, wherein rather than optimising the input signal based on known faults, the signal is optimised to take into account variations in values of functional specifications.

22. A method as claimed in any of the preceding claims, wherein the step of optimising the digital test input is implemented using an optimisation algorithm, for example a hill-climbing algorithm and/or a genetic algorithm or modified version of one of these.

23. A digital test signal or a copy thereof for testing analogue or mixed signal circuits that is a product of the method of any of claims 1 to 22.

24. A system for improving digital testing of an analogue or mixed-signal circuit, the system comprising means for optimising an input digital test signal, preferably wherein the means for optimising comprise an optimisation algorithm, such as a hill-climbing algorithm and/or a genetic algorithm or a modified version of one of these.

25. A system as claimed in claim 24, wherein the means for optimising comprise means for applying a plurality of different digital inputs to a fault free circuit and a

faulty circuit, preferably software-based simulations of the fault free and faulty circuits; means for monitoring the corresponding outputs of the fault free and the faulty circuits for each input, and means for selecting an improved test input as part of an optimisation procedure.

26. A system as claimed in claim 25 comprising means for determining a measure, for example a figure of merit, that is indicative of differences between an output of a fault free circuit and an output of known faulty circuit in response to a digital input signal, wherein the means for selecting the optimum input test signal is operable to do so based on the measures determined for each input digital signal.

27. A system as claimed in any of claims 24 to 26, wherein the means for applying a plurality of digital input signals are operable to apply an initial signal and then vary that according to pre-determined criteria.

28. A system as claimed in claim 27, wherein the means for applying are operable to vary the initial input digital signal by changing the length of one or more individual pulses in that signal.

29. A system as claimed in claim 28, wherein the means for applying are operable to vary the pulse length by the same amount or by increasingly large or small amounts or by different amounts, which different amounts may be selected randomly or by predefined scheme.

30. A system as claimed in any of claims 24 to 29, wherein the means for applying are operable to vary the frequency of the input digital signal.

31. A system as claimed in any of claims 24 to 30 wherein the means monitoring are operable to monitor analogue outputs from the fault free and faulty circuits.

32. A system as claimed in any of claims 24 to 31 wherein the means monitoring are operable to monitor digital outputs from the fault free and faulty circuits.

33. A system as claimed in any of claims 24 to 32 further comprising means for determining a figure of merit for each one of a plurality of different faulty circuits and determining a composite figure of merit combining all of these.

34. A system for improving digital testing of an analogue or mixed-signal circuit, the system being configured to optimise a digital input signal.

35. A method for testing analogue and/or mixed-signal circuits using a digital signal, the method comprising applying to the circuit under test an optimised test signal as claimed in claim 23; comparing an output of the circuit under test with an expected output for a fault free circuit and determining a fault based on a result of the step of comparing.

36. A method as claimed in claim 35, wherein the output from the circuit under test and the expected output are analogue.

37. A method as claimed in claim 36 further involving digitising the output of the circuit under test, wherein

the step of comparing may involve comparing digitised outputs.

38. A method as claimed in any of claims 35 to 37, wherein the expected output for the fault free circuit includes an acceptable tolerance range for the optimised input test signal.

39. A method as claimed in any of claims 35 to 38 further comprising storing outputs for one or more known faults for the optimised digital test signal and comparing an output from a circuit under test with these.

40. A method as claimed in claim 39, wherein the stored outputs for the one or more known faults include an acceptable tolerance range for the optimised input test signal.

41. A method as claimed in any of claims 35 to 40 wherein in the event that the gain of the circuit is to be tested, the digital test signal has an optimised offset voltage and/or amplitude.

42. A system for testing analogue and/or mixed-signal circuits using a digital signal, the system comprising means for applying to the circuit under test an optimised test signal as defined in claim 23; means for comparing an output of the CUT with an expected output for a good circuit and means for determining a fault based on an output from the means for comparing.

43. A system as claimed in claim 42, wherein the outputs from the CUT are analogue.

44. A system as claimed in claim 43, wherein means are provided for digitising the outputs of the circuit under test and the means for comparing are operable to compare the digitised outputs.

45. A system as claimed in any of claims 42 to 44 wherein a single digital signal generator is provided for stimulating a plurality of different electronic functions or sub-systems.

46. A system as claimed in claim 45, wherein the means for determining a fault comprise a single detector that is operable to analyse output signals from each of the plurality of different electronic functions or sub-systems.

47. A computer program for improving testing of an analogue or mixed-signal circuit using a digital signal, the computer program being provided preferably on a data carrier or computer readable medium and having code or instructions for optimising an input digital test signal.

48. A computer program as claimed in claim 45 having code or instructions for applying a plurality of different digital inputs to a fault free circuit and a faulty circuit, preferably software-based simulations of the fault free and faulty circuits; monitoring the corresponding outputs of the fault free and the faulty circuits for each input, and selecting an optimum digital input using the outputs produced for each input.

49. A computer program as claimed in claim 48 comprising code or instructions for determining, for each digital input signal, a measure, for example a figure of merit,

that is indicative of differences between an output of a fault free circuit and an output of known faulty circuit in response to a digital input signal and selecting an optimum input test signal based on the determined measures for each input digital signal.

50. A computer program may as claimed in claim 47 or claim 48 or claim 49 having code or instructions for modelling output responses for the fault free and faulty circuits.

51. A computer program for use in a method of testing an analogue or mixed-signal circuit using a digital signal, the computer program being provided preferably on a data carrier or computer readable medium and having code or instructions for applying to a circuit under test a test signal as determined using the method defined in claims 1 to 22; comparing an output of the circuit under test with an expected output for a good circuit and determining whether there is a fault based on an output from the means for comparing.

52. A computer program as claimed in claim 51 having code or instructions for storing a measure, for example a figure of merit, for a circuit having a known fault and comparing the measure for the circuit under test with that for the known fault.

53. A test system that includes means for generating an optimised digital test signal as determined using the method defined in claims 1 to 22 or as set out in claim 23, means for applying the digital test signal to an analogue or mixed-signal circuit under test, means for comparing an output of the circuit under test with an expected output for a known circuit, for example a fault

free circuit or a known faulty circuit, which is also stored or generated locally, and means for determining a fault based on an output from the means for comparing.

54. A test system as claimed in claim 53 that is provided on the same chip as the circuit under test.

55. An electronic device, such as a mobile telephone, that includes a test system that has means for generating an optimised digital test signal as determined using the method as claimed in any of claims 1 to 22, means for applying the digital test signal to an analogue or mixed-signal circuit under test, means for comparing an output of the circuit under test with an expected output for a good circuit, which is also stored or generated locally, and means for determining a fault based on an output from the means for comparing.